

What is claimed is:

1. A semiconductor chip with a rectangular main surface comprising:
 - a first side composing said main surface;
 - 5 a second side opposed to said first side;
 - a main electrode pad group composed of a plurality of main electrode pads, which plurality of main electrode pads is arranged on said main surface along said first side;
 - 10 a first electrode pad group composed of a plurality of first electrode pads, which plurality of first electrode pads is arranged between said first side and said main electrode pad group;
 - a second electrode pad group composed of a plurality of second electrode pads, which plurality of second electrode pads is arranged on said main surface along said second side;
 - 15 a first interconnection connecting said main electrode pad with said first electrode pad; and
 - a second interconnection connecting said main electrode pad with said second electrode pad.
- 20
2. The semiconductor chip according to claim 1, wherein said first interconnection and said second interconnection are provided on said main surface of said semiconductor chip.
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3. The semiconductor chip according to claim 1,

wherein said first interconnection and said second interconnection are provided within said semiconductor chip.

5 4. The semiconductor chip according to claim 3,
wherein any one or both of said first interconnection
and said second interconnection has or have a multi-layer
wired structure.

10 5. A semiconductor chip with a rectangular main
surface comprising:
 a first side composing said main surface;
 a second side opposed to said first side;
 a main electrode pad group composed of a plurality of
15 main electrode pads, which plurality of main electrode pads
is arranged on said main surface along said first side;
 a first electrode pad group composed of a plurality of
first electrode pads, which plurality of first electrode
pads is arranged between said first side and said main
20 electrode pad group;
 a second electrode pad group composed of a plurality
of second electrode pads, which plurality of second
electrode pads is arranged on said main surface along said
second side;
25 a plurality of conversion type interconnection
connecting said main electrode pad with said first
electrode pad one-on-one, which plurality of conversion

type interconnection is provided on said main surface not in parallel with said main electrode pad group and said first electrode pad group; and

a plurality of second interconnections connecting said

5 main electrode pad with said second electrode pad one-on-one, said plurality of second interconnections is arranged on said first main surface.

6. A semiconductor chip with a rectangular main

10 surface comprising:

a first side composing said main surface;

a second side opposed to said first side;

a main electrode pad group composed of a plurality of main electrode pads, which plurality of main electrode pads

15 is arranged on said main surface along said first side and has an area that is sufficiently wide so that two bonding wires can be connected thereto, respectively;

a second electrode pad group composed of a plurality of second electrode pads, which plurality of second

20 electrode pads is arranged on said main surface along said second side; and

a second interconnection connecting said main electrode pad with said second electrode pad one-on-one.

25 7. The semiconductor chip according to claim 6,

wherein said main electrode pad is formed in a rectangular shape and has a sufficiently wide area so that,

two bonding wires can be connected thereto;

a longer direction of said rectangular shape is elongated in a direction orthogonal to said first side; and said main electrode pad is separated into a first partial main electrode pad at said first side, to which one of said bonding wires is connected, and a second partial main electrode pad, to which the other one of said bonding wires is connected.

10 8. The semiconductor chip according to claim 7,
wherein said main electrode pad further includes a connection area connecting said first partial main electrode pad with said second partial main electrode pad so that a width in a direction orthogonal to the direction in which said main electrode pad is elongated is narrower than the widths of said first and second partial electrode pads.

20 9. The semiconductor chip according to claim 8,
wherein said second electrode pad is formed in a rectangular shape and has an area to which two bonding wires can be connected;

25 a longer direction of said rectangular shape is elongated in a direction orthogonal to said second side; and

said second electrode pad is separated into a first partial electrode pad at said second side, to which one of

said bonding wires is connected, and a second partial electrode pad, which adjoins said first partial electrode pad and to which the other one of said bonding wires is connected.

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10. The semiconductor chip according to claim 9,
wherein the number of said first electrode pads is
less than the number of said main electrode pads, and said
first interconnection is connected to an electrode pad
10 which is different from the electrode pad, to which said
second interconnection is connected, from among said
plurality of main electrode pads.

15 11. The semiconductor chip according to claim 10,
wherein, in said main electrode pad group, an
electrode pad, to which said first interconnection is
connected, and an electrode pad, to which said second
interconnection is connected, are alternately arranged.

20 12. The semiconductor chip according to claim 9,
wherein an interconnection connecting said main
electrode pads with said second electrode pads of the same
number as said main electrode pads one by one is provided.

25 13. The semiconductor chip according to claim 1,
wherein any one or both of said first and second
interconnections is or are formed within the same wired

layer.

14. The semiconductor chip according claim 1,
wherein said semiconductor chip is provided with a
multi-layer wired structure; and
any one or both of said first and second
interconnections has or have a multi-layer wired structure
to which a plurality of wired layer is connected through a
via in which a via hole is embedded.

10 15. The semiconductor chip according to claim 1,
wherein circuit elements having weak tolerance to the
stress are integrated in the vicinity of the lower side of
said main electrode pad group.

15 16. A semiconductor device comprising:
a substrate having a main surface having a first range
on which a first bonding pad is formed, a second range on
which a second bonding pad is formed, and a third range
existing between said first range and said second range;
20 a plurality of semiconductor chips with the same
configuration to be laminated in said third range of said
main surface or to be further mounted in the other
semiconductor chip laminated in said third range; each of
said plural semiconductor chips with a rectangular main
25 surface having a first side composing said main surface; a
second side opposed to said first side; a main electrode
pad group composed of a plurality of main electrode pads,

which plurality of main electrode pads is arranged on said main surface along said first side; a first electrode pad group composed of a plurality of first electrode pads, which plurality of first electrode pads is arranged between 5 said first side and said main electrode pad group; a second electrode pad group composed of a plurality of second electrode pads, which plurality of second electrode pads is arranged on said main surface along said second side; a first interconnection connecting said main electrode pad 10 with said first electrode pad; and a second interconnection connecting said main electrode pad with said second electrode pad;

a first bonding wire electrically connecting said first bonding pad with said first electrode pad;

15 a second bonding wire electrically connecting said main electrode pad of said semiconductor chip with a first electrode pad of the other semiconductor chip to be mounted on said semiconductor chip;

a third bonding wire electrically connecting said main 20 electrode pad of said semiconductor chip with a main electrode pad of the other semiconductor chip to be mounted on said semiconductor chip; and

a fourth bonding wire electrically connecting said second bonding wire with said second electrode pad;

25 wherein, in said plural semiconductor chips, said each first side is located at the same side, each main surface is turned in the same direction, and said main electrode

pad and said first electrode pad of said semiconductor chip located at the lower side are located at the outside from the first side of said other semiconductor chip located at the upper side and said plural semiconductor chips are
5 laminated each other.

17. A semiconductor device comprising:

a substrate having a main surface having a first range on which a first bonding pad is formed, a second range on
10 which a second bonding pad is formed, and a third range existing between said first range and said second range;

a plurality of semiconductor chips with the same configuration to be laminated in said third range of said main surface or to be further mounted in the other
15 semiconductor chip laminated in said third range; each of said plural semiconductor chips with a rectangular main surface having a first side composing said main surface; a second side opposed to said first side; a main electrode pad group composed of a plurality of main electrode pads,
20 which plurality of main electrode pads is arranged on said main surface along said first side; a first electrode pad group composed of a plurality of first electrode pads, which plurality of first electrode pads is arranged between said first side and said main electrode pad group; a second
25 electrode pad group composed of a plurality of second electrode pads, which plurality of second electrode pads is arranged on said main surface along said second side; a

plurality of conversion type interconnections electrically connecting said main electrode pad with said first electrode pad one-on-one, said plurality of conversion type interconnection is provided on said main surface not in parallel with said main electrode pad group and said first electrode pad group; and

a plurality of second interconnections electrically connecting said main electrode pad with said second electrode pad one-on-one;

10 a first bonding wire electrically connecting said first bonding pad with said first electrode pad;
a second bonding wire electrically connecting said main electrode pad of said semiconductor chip with a main electrode pad of the other semiconductor chip to be mounted
15 on said semiconductor chip; and

a third bonding wire electrically connecting said second bonding wire with a second electrode pad of said other semiconductor chip;

wherein, in said plural semiconductor chips, said each
20 first side is located at the same side, each main surface is turned in the same direction, and said main electrode pad and said first electrode pad of said semiconductor chip located at the lower side are located at the outside from the first side of said other semiconductor chip located at
25 the upper side and said plural semiconductor chips are laminated each other.

18. A semiconductor device comprising:

a substrate having a main surface having a first range on which a first bonding pad is formed, a second range on which a second bonding pad is formed, and a third range existing between said first range and said second range;

5 a plurality of semiconductor chips with the same configuration to be laminated in said third range of said main surface or to be further mounted in the other semiconductor chip laminated in said third range; each of

10 said plural semiconductor chips with a rectangular main surface wherein a longer direction of said rectangular shape is elongated in a direction orthogonal to said first side; having a first side composing said main surface; a second side opposed to said first side; an area

15 sufficiently wide so that two bonding wires arranged on said main surface along said first side can be connected thereto; a main electrode pad group composed of a plurality of main electrode pads, which plurality of main electrode pads is separated into a first partial electrode pad at

20 said first side and a second partial electrode pad; a second electrode pad group composed of a plurality of second electrode pads, which plurality of second electrode pads is arranged on said main surface along said second side; and a plurality of second interconnections

25 electrically connecting said main electrode pad with said second electrode pad one-on-one;

a first bonding wire electrically connecting said

first bonding pad with said first partial main electrode pad;

a second bonding wire electrically connecting said second partial main electrode pad of said semiconductor chip with a first partial main electrode pad of the other semiconductor chip to be mounted on said third range of said semiconductor chip;

10 a third bonding wire electrically connecting said second partial main electrode pad of said semiconductor chip with a second partial main electrode pad of the other semiconductor chip to be mounted on said third range of said semiconductor chip; and

15 a fourth bonding wire electrically connecting said second bonding pad with a second electrode pad of said other semiconductor chip;

wherein, in said plural semiconductor chips, said each first side is located at the same side, each main surface is turned in the same direction, and said main electrode pad and said first electrode pad of said semiconductor chip 20 located at the lower side are located at the outside from the first side of said other semiconductor chip located at the upper side and said plural semiconductor chips are laminated each other.

25 19. The semiconductor device according to claim 18, wherein said main electrode pad of said semiconductor chip further includes a connection area connecting said

first partial main electrode pad with said second partial main electrode pad so that a width in a direction orthogonal to the direction in which said main electrode pad is elongated is narrower than the widths of said first and second partial electrode pads.

20. A semiconductor device comprising:

a substrate having a main surface having a first range on which a first bonding pad is formed, a second range on 10 which a second bonding pad is formed, and a third range existing between said first range and said second range;

a first semiconductor chip to be laminated in said third range of said main surface; said first semiconductor chip with a rectangular main surface wherein a longer

15 direction of said rectangular shape is elongated in a direction orthogonal to said first side; having a first side composing said main surface; a second side opposed to said first side; an area sufficiently wide so that two bonding wires arranged on said main surface along said

20 first side can be connected thereto; a main electrode pad group composed of a plurality of main electrode pads, which plurality of main electrode pads is separated into a first partial main electrode pad at said first side and a second partial main electrode pad; a second electrode pad group

25 composed of a plurality of second electrode pads, which plurality of second electrode pads is arranged on said main surface along said second side; and a plurality of second

interconnections electrically connecting said main electrode pad with said second electrode pad one-on-one;

a second semiconductor chip having the same configuration as that of said first semiconductor chip,

5 which is mounted on said first semiconductor chip;

a third semiconductor chip having the same configuration as those of said first and second semiconductor chips, which are mounted on said second semiconductor chip;

10 a first bonding wire connecting said first partial main electrode pad of said first semiconductor chip with said first bonding pad of said substrate;

a second bonding wire connecting said second partial main electrode pad of said first semiconductor chip with a

15 first partial main electrode pad of said second semiconductor chip;

a third bonding wire connecting said second partial main electrode pad of said second semiconductor chip with a first partial main electrode pad of said third semiconductor chip; and

20 a fourth bonding wire connecting said second electrode pad of said third semiconductor chip with said second bonding pad of said substrate;

wherein, in said plural semiconductor chips, said each

25 first side is located at the same side, each main surface is turned in the same direction, and said main electrode pad and said first electrode pad of said semiconductor chip

located at the lower side are located at the outside from the first side of said other semiconductor chip located at the upper side and said plural semiconductor chips are laminated each other.

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21. The semiconductor device according to claim 20, wherein said second electrode pad further includes a connection area connecting said first partial electrode pad with said second partial electrode pad so that a width in a direction orthogonal to the direction in which said main electrode pad is elongated is narrower than the widths of said first and second partial electrode pads.

22. A semiconductor device comprising:

15 a substrate having a main surface having a first range on which a first bonding pad is formed, a second range on which a second bonding pad is formed, and a third range existing between said first range and said second range; a first semiconductor chip to be laminated in said
20 third range of said main surface; said first semiconductor chip with a rectangular main surface wherein a longer direction of said rectangular shape is elongated in a direction orthogonal to said first side; having a first side composing said main surface; a second side opposed to
25 said first side; an area sufficiently wide so that two bonding wires arranged on said main surface along said first side can be connected thereto; a main electrode pad

group composed of a plurality of main electrode pads, which plurality of main electrode pads is separated into a first partial main electrode pad at said first side and a second partial main electrode pad; wherein a longer direction of

5 said rectangular shape is elongated in a direction orthogonal to said second side; having an area sufficiently wide so that two bonding wires arranged on said main surface along said second side can be connected thereto; a second electrode pad group composed of a plurality of

10 second electrode pads, which plurality of second electrode pads is separated into a first partial electrode pad at said second side and a second partial electrode pad; and a plurality of second interconnections connecting said main electrode pad with said second electrode pad one-on-one;

15 a second semiconductor chip having the same configuration as that of said first semiconductor chip, which is mounted on said third semiconductor chip;

20 a third semiconductor chip having the same configuration as those of said first and second semiconductor chips, which is mounted on said first semiconductor chip;

25 a fourth semiconductor chip having the same configurations as those of said first, second, and third semiconductor chips, which is mounted on said second semiconductor chip;

30 a fifth semiconductor chip having the same configurations as those of said first, second, third and

fourth semiconductor chips, which is mounted across said third and fourth semiconductor chips;

a first bonding wire connecting said first partial main electrode pad of said first semiconductor chip with
5 said first bonding pad of said substrate;

a second bonding wire connecting said second partial main electrode pad of said first semiconductor chip with a first partial main electrode pad of said third semiconductor chip;

10 a third bonding wire connecting said second partial main electrode pad of said third semiconductor chip with a first partial main electrode pad of said fifth semiconductor chip;

a fourth bonding wire connecting said first partial electrode pad of said fifth semiconductor chip with said second partial electrode pad of said fourth semiconductor chip;
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a fifth bonding wire connecting said first partial electrode pad of said fourth semiconductor chip with said second partial electrode pad of said second semiconductor chip; and
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a sixth bonding wire connecting said first partial electrode pad of said second semiconductor chip with said second bonding pad of said substrate;

25 wherein said first and second semiconductor chips are laminated in said third range with said each first side located serially at the same side, each main surface is

turned in the same direction; said third and fourth semiconductor chips are laminated with said main electrode pad and said first electrode pad of said first and second semiconductor chips located at the lower side are located
5 at the outside from the first side of said other semiconductor chip located at the upper side; and said fifth chip is laminated with said main electrode and said first electrode pad of said third chip and said second electrode pad of said fourth semiconductor chip exposed.

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23. The semiconductor device according to claim 22,
wherein said main electrode pad further includes a connection area connecting said first partial main electrode pad with said second partial main electrode pad
15 so that a width in a direction orthogonal to the direction in which said main electrode pad is elongated is narrower than the widths of said first and second partial electrode pads.

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24. The semiconductor device according to claim 23,
wherein said second electrode pad further includes a connection area connecting said first partial main electrode pad with said second partial main electrode pad so that a width in a direction orthogonal to the direction
25 in which said second electrode pad is elongated is narrower than the widths of said first and second partial electrode pads.

25. The semiconductor chip according to claim 22,
wherein an interconnection connecting said main
electrode pads with said second electrode pads of the same
5 number as said main electrode pads one by one is provided.

26. The semiconductor chip according to claim 16,
wherein circuit elements having weak tolerance to the
stress are integrated in the vicinity of the lower side of
10 said main electrode pad group.

27. The semiconductor chip according to claim 16,
wherein said substrate is provided with a via hole
passing through from said first surface to said second
15 surface, a via connected to said plurality of first and
second bonding pads having said via hole embedded therein,
and an external terminal connected to said via; and said
substrate is further provided with a sealing portion
sealing all bonding wires on said substrate.